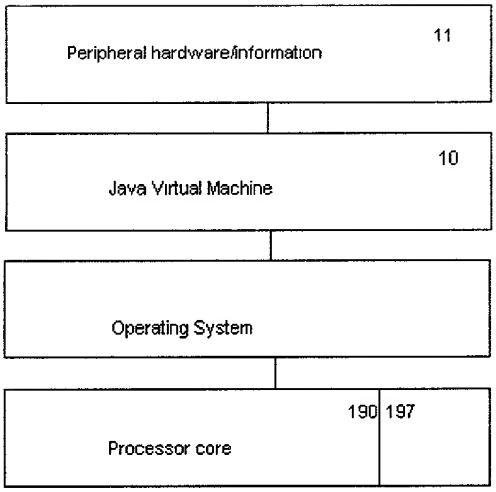

Figure 1

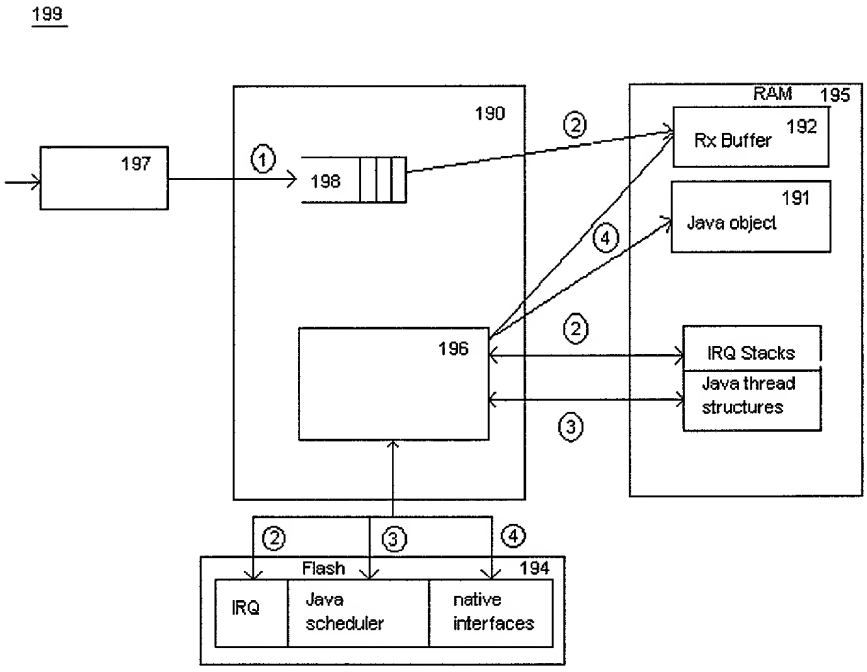

Figure 2

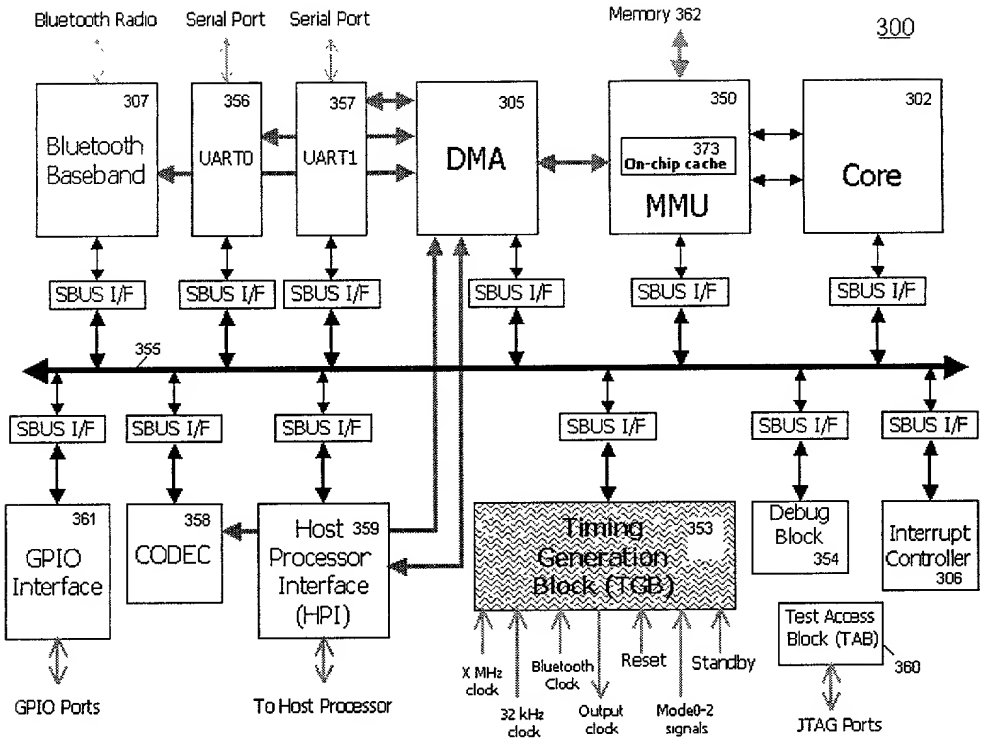
Bluetooth Radio
Serial Port
Serial Port
Memory 362
300
307
Bluetooth Baseband
356
UART0
357
UART1
305
DMA
350
373
On-chip cache
MMU
302
Core
SBUS I/F
355
361
GPIO Interface
358
CODEC
Host 359 Processor Interface (HPI)
Timing Generation Block (TGB) 353
Debug Block 354
Interrupt Controller 306
Test Access Block (TAB) 360
GPIO Ports
To Host Processor
X MHz clock
32 kHz clock
Bluetooth Clock
Output clock
Reset
Mode0-2 signals
Standby
JTAG Ports

Figure 3a

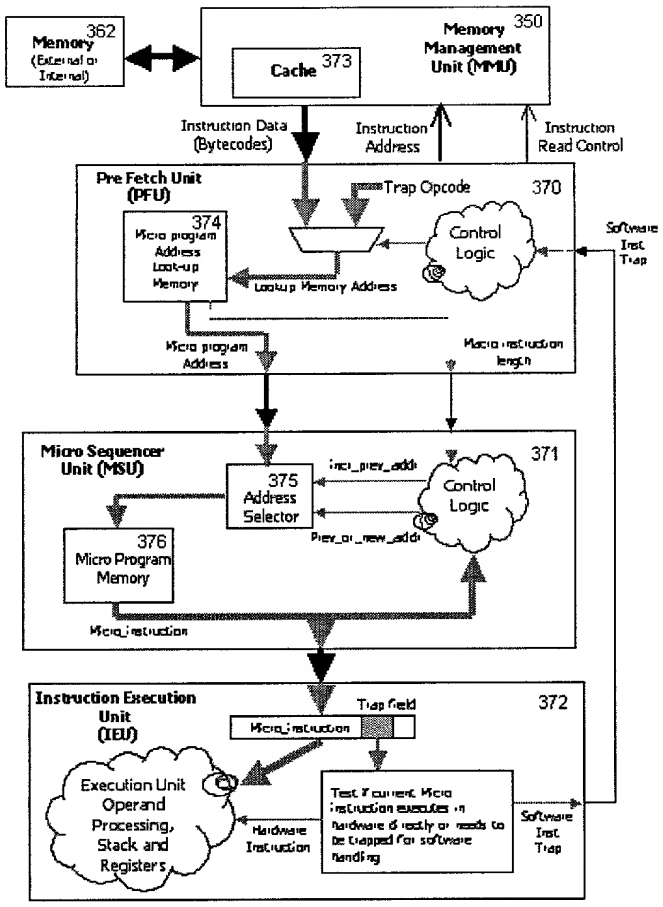

Figure 3b

Upon a trapped instruction which is not directly executed in hardware:

1) Current Opcode is loaded into a register used to handle vector table bases (in IEU)
2) Some registers are swapped
3) Some registers are pushed onto the stack
4) Software execution transfers via the vector table setting
5) Current opcode is translated via software into a sequence of opcodes that can be executed directly in hardware
6) This opcode sequence is then executed in place of the current opcode

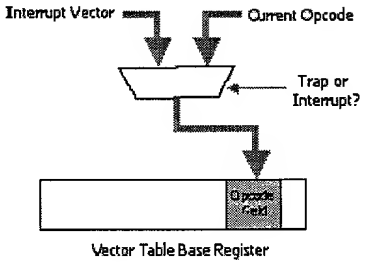

Figure 3c

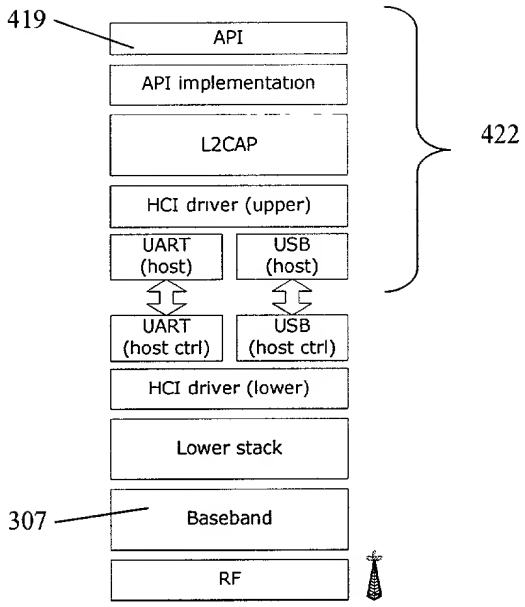
419
API
API implementation
L2CAP
HCI driver (upper)
UART (host)
USB (host)
422
UART (host ctrl)
USB (host ctrl)
HCI driver (lower)
Lower stack
307
Baseband
RF

Figure 4

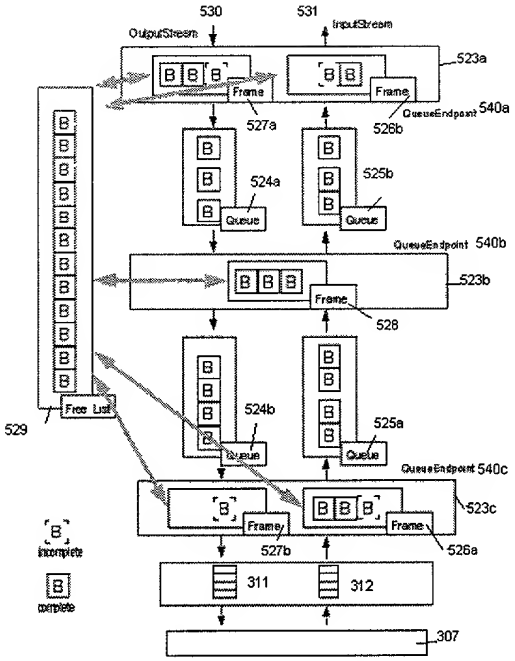

Figure 5

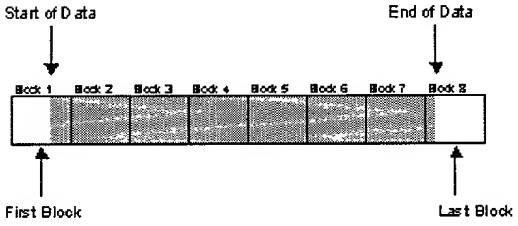

Figure 6a

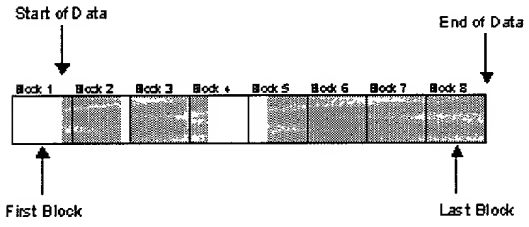

Figure 6b

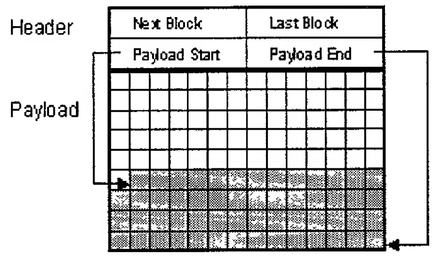

Figure 6c

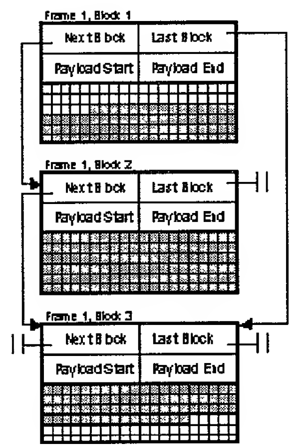

Figure 6d

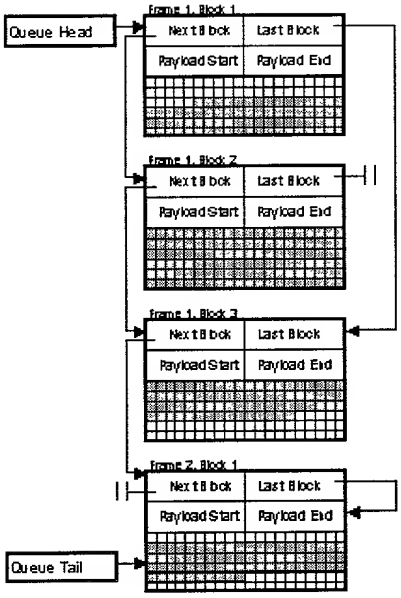

Figure 6e

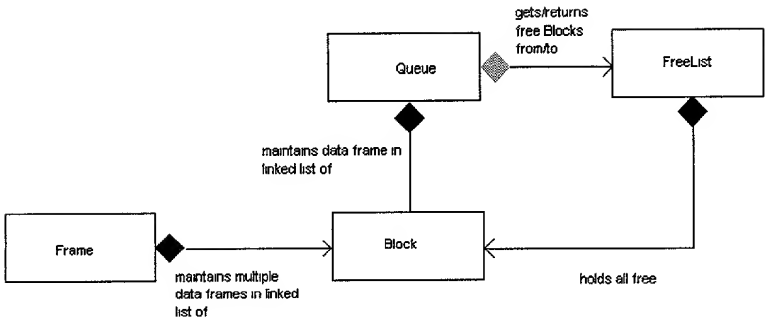

Figure 7a

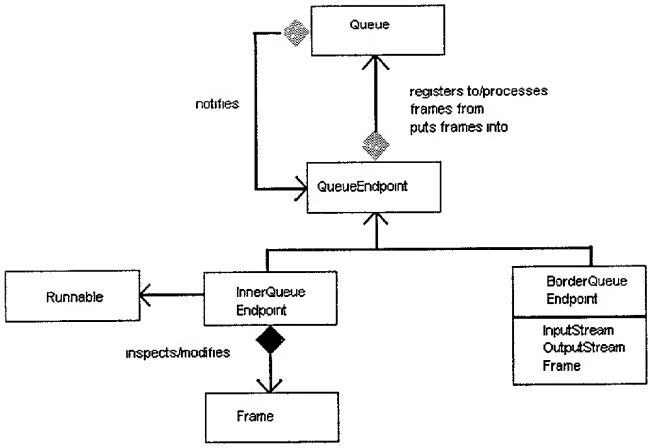

Figure 7b

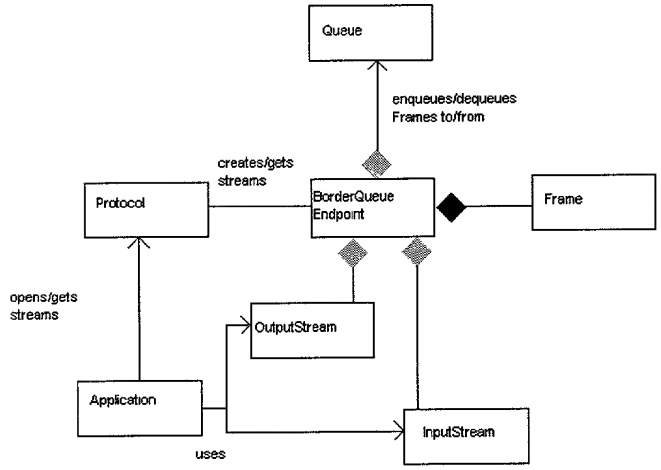

Figure 7c

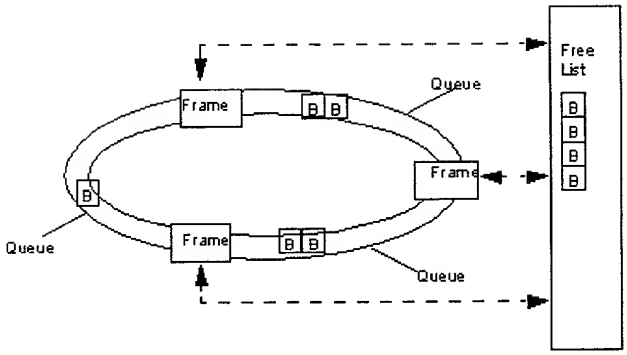

Figure 8

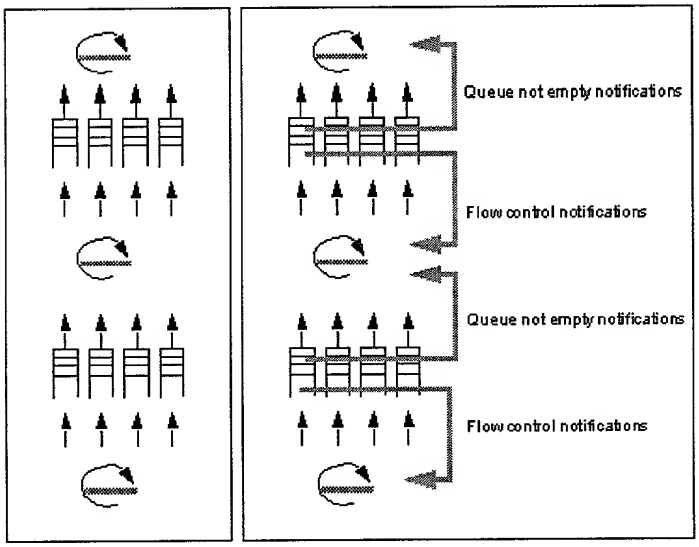

Figure 9

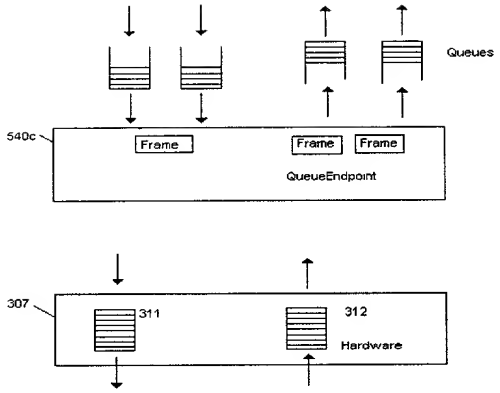

Figure 10

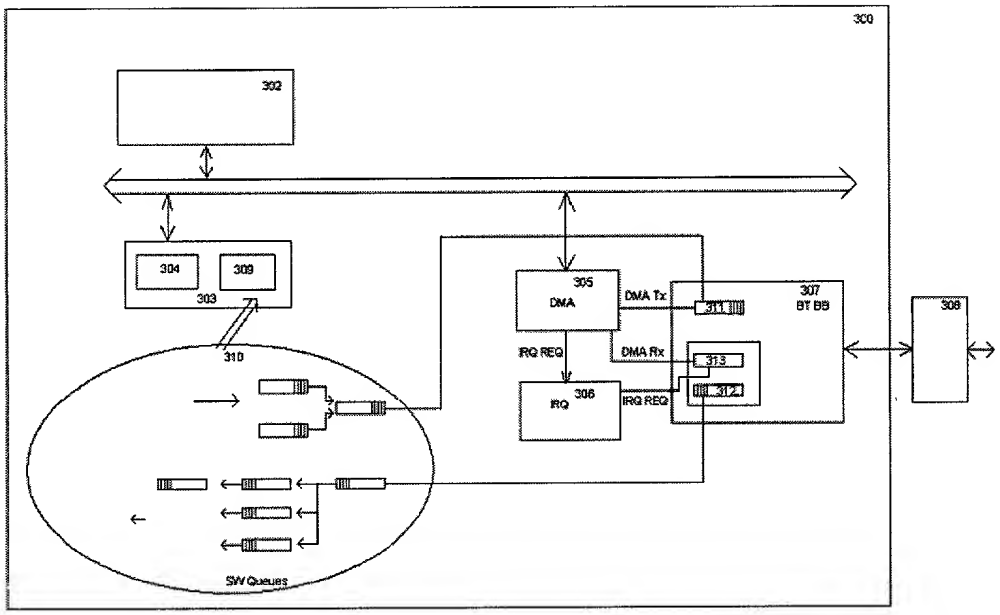

Figure 11

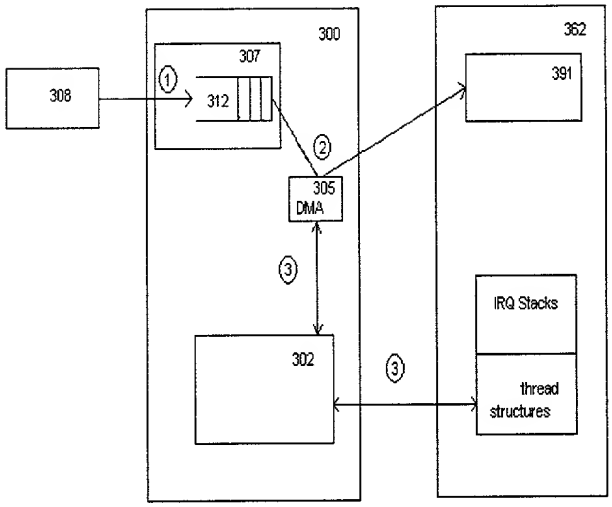
300
307
308
312
362
391
305
DMA
IRQ Stacks
302
thread
structures

Figure 12

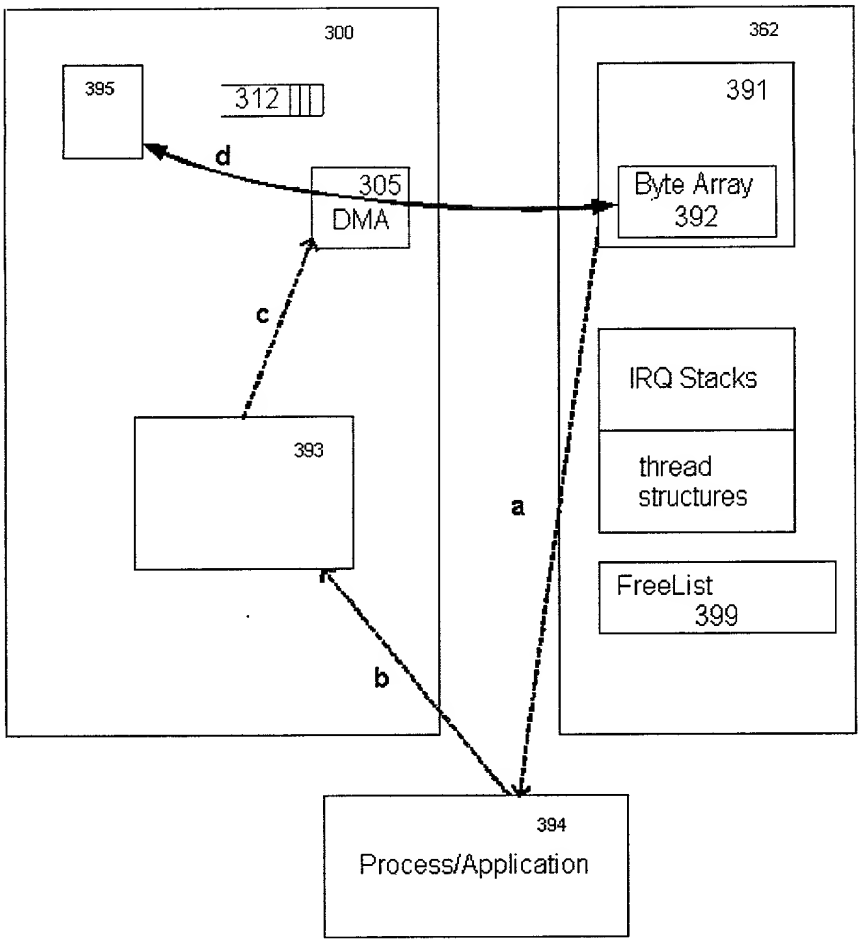
300
362
395
312
391
d
305
DMA
Byte Array
392
c
IRQ Stacks
393
thread
structures
a
FreeList
399
b
394
Process/Application

Figure 13